UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,184	10/30/2001	Frederic Reblewski	109894-129746	4114

22907 7590 08/24/2005

BANNER & WITCOFF
1001 G STREET N W
SUITE 1100
WASHINGTON, DC 20001

EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,184	REBLEWSKI, FREDERIC	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,7,8,11,12,14,19,20,24,30 and 32-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7,8,11,12,14,19,20,24,30 and 32-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *15 July 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Response mailed on June 10, 2005. Claims 1, 5, 7, 11, 14, 19, 24, 30, 32, 33 and 34 were amended. Claims 4, 6, 9-10, 13, 15-18, 21-23, 25-29 and 31 were deleted. Claims 1-3, 5, 7, 8, 11, 12, 14, 19, 20, 24, 30 and 32-34 of the application are pending. This office action is made non-final.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statements filed on July 15 2005 together with copies of the patents and papers. The patents and papers have been considered.

Specification

3. The disclosure is objected to because of the following informalities:

Specification Page 3, Line 15, "The present invention includes the consitution of an emulation system" appears to be incorrect and it appears that it should be "The present invention includes the constitution of an emulation system".

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-3, 5, 7-8 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5.1 Claim 1 states in part, "locally retrieve from said emulation ICs state data of emulation state circuit elements". How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

5.2 Claim 2 states in part, "local retrieval of state data of the emulation state circuit elements". How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

5.3 Claim 7 states in part, "locally retrieving from emulation ICs of said logic board state data of emulation state circuit elements of a partition of an IC design being emulated". How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

5.4 Claim 30 states in part, "locally retrieving on said emulation IC, using on-chip data processing resources, emulation state circuit elements of a partition of an IC design being emulated;

locally analyzing state data of the emulation state circuit elements".

What is meant by retrieving emulation state circuit elements? The circuit elements are hardware elements. How does one retrieve the hardware elements during emulation? How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

7. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-3, 5, 7, 8, 11, 12, 14, 19, 20, 24, 30 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Quayle et al.** (U.S. Patent 6,694,464) in view of **Vries et al.** ("Built-in self-test methodology for A/D converters", IEEE 1997).

8.1 **Quayle et al.** teaches method and apparatus for dynamically testing electrical interconnect. Specifically, as per claim 1, **Quayle et al.** teaches a logic board designed for circuit emulation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising

a plurality of input/output (I/O) pins (Abstract, L8-9; CL4, L27-30; CL16, L62-64);

a plurality of emulation integrated circuits (IC), each having reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of a partition of an IC design (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13); and

a plurality of on-board data processing resources coupled to the emulation ICs (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26) to locally retrieve from the emulation ICs state data of emulation state circuit elements (CL18, L5-9; CL23, L63-65), responsive to a monitor and report request received through the I/O pins (CL5, L2-4; Fig.20a, Item 238), and to locally analyze the retrieved state data to detect occurrence of one or more events, as well as report on the occurrence of the one or more events upon their detection through the I/O pins (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59);

wherein the on-board data processing resources are further employed to locally generate a plurality of testing stimuli, and locally apply the locally generated testing stimuli to the partition of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to a testing request received through the I/O pins (Fig. 19, BP clocks).

Quayle et al. does not expressly teach that at least one of the emulation ICs comprises on-chip data processing resources to cooperate and assist the onboard data processing resources to perform the local generation and application of testing stimuli. **Vries et al.** teaches that at least one of the emulation ICs comprises on-chip data processing resources to cooperate and assist the onboard data processing resources to perform the local generation and application of testing stimuli (Page 353, CL1, Para 4, L3-5; Page 353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the logic board of **Quayle et al.** with the logic board of **Vries et al.** that included at least one of the emulation ICs comprising on-chip data processing resources to cooperate and assist the onboard data processing resources to perform the local generation and application of testing stimuli. The artisan would have been motivated because the amount of test data to be processed by the tester would be reduced by means of on-chip processing reducing the overall test time; and that would reduce the test costs an IC design.

In addition, **Azais et al.** ("A low-cost adaptive ramp generator for analog BIST applications", IEEE, March 2001) teaches on-chip test stimuli generation and on-chip testing of mixed signal circuits (See Page 266, CL1, Para 3 to CL2, Para 1).

Per claim 2: **Quayle et al.** teaches that the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the responsive local retrieval of state data of the emulation state circuit elements (CL18, L5-9; CL23, L63-65), local analysis of the retrieved state data, and reporting of event detection (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59), and a processor coupled to the storage medium to execute the programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206).

Per claim 3: **Quayle et al.** teaches that at least one of the emulation ICs comprises on-chip data processing resources (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18), to cooperate and assist the on-board data processing resources to perform the local monitoring and reporting of monitored events (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Per claim 5: **Quayle et al.** teaches that the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic

board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the responsive local generation and application of stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), and a processor coupled to the storage medium to execute the programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206).

8.2 As per claim 7, **Quayle et al.** teaches in an emulation apparatus, a method of operation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising:

receiving by an emulation logic board, through input/output (I/O) pins of the logic board, a monitor and report request (CL5, L2-4; Fig.20a, Item 238);

in response, locally retrieving from emulation ICs of the logic board state data of emulation state circuit elements of a partition of an IC design being emulated (CL18, L5-9; CL23, L63-65);

locally analyzing the retrieved state data to detect occurrence of one or more events (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59); and

reporting through the I/O pin, of the logic board occurrence of the one or more events, upon detection of their occurrence (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59);

wherein the method further comprises locally generating on the logic board a plurality of testing stimuli, and applying the locally generated testing stimuli to emulation circuit elements of a respective emulation IC corresponding to the partition of the IC design being emulated (CL22,

L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to an external testing request received by the logic board through the I/O pins of the logic board (Fig. 19, BP clocks).

Quayle et al. does not expressly teach that at least some of the generation of testing stimuli are performed by on-chip data processing resources of the emulation ICs. **Vries et al.** teaches that at least some of the generation of testing stimuli are performed by on-chip data processing resources of the emulation ICs (Page 353, CL1, Para 4, L3-5; Page 353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **Quayle et al.** with the method of **Vries et al.** that included at least some of the generation of testing stimuli being performed by on-chip data processing resources of the emulation ICs. The artisan would have been motivated because the amount of test data to be processed by the tester would be reduced by means of on-chip processing reducing the overall test time; and that would reduce the test costs of an IC design.

Per claim 8: **Quayle et al.** teaches that at least some of the analysis and detection are performed by on-chip data processing resources of the emulation ICs, in lieu of retrieving the state data from the emulation ICs (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18), and then analyzing the state data to detect for the one or mare events (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

8.3 As per claim 11, **Quayle et al.** teaches a logic board designed for circuit emulation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising

a plurality of input/output (I/O) pins (Abstract, L8-9; CL4, L27-30; CL16, L62-64);

a plurality of emulation integrated circuits (IC), each having reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of a partition of an IC design (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13); and

a plurality of on-board data processing resources coupled to the emulation ICs to locally generate a plurality of testing stimuli, and locally apply the locally generated testing stimuli to emulation circuit elements of a respective emulation IC corresponding to the partition of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to a testing request received through the I/O pins (Fig. 19, BP clocks).

Quayle et al. does not expressly teach that at least one of the emulation ICs comprises on-chip data processing resources to cooperate with and assist the onboard data processing resources to perform the local generation and application of testing stimuli. **Vries et al.** teaches that at least one of the emulation ICs comprises on-chip data processing resources to cooperate with and assist the onboard data processing resources to perform the local generation and application of testing stimuli (Page 353, CL1, Para 4, L3-5; Page 353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9). It would have been obvious to one of ordinary skill in the art at

the time of Applicant's invention to modify the logic board of **Quayle et al.** with the logic board of **Vries et al.** that included at least one of the emulation ICs comprising on-chip data processing resources to cooperate with and assist the onboard data processing resources to perform the local generation and application of testing stimuli. The artisan would have been motivated because the amount of test data to be processed by the tester would be reduced by means of on-chip processing reducing the overall test time; and that would reduce the test costs an IC design.

Per claim 12: **Quayle et al.** teaches that the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the responsive local generation and application of stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), and a processor coupled to the storage medium to execute the programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206).

8.4 As per claim 14, **Quayle et al.** teaches in an emulation apparatus, a method of operation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising:

receiving by a logic board, through input/output (I/O) pins of the logic board, a testing request (Fig. 19, BP clocks);

in response, locally generating on the logic board a plurality testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65); and

locally applying the locally generated testing stimuli to emulation circuit elements of an emulation IC corresponding to a partition of an IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

Quayle et al. does not expressly teach that at least some of the generation of testing stimuli are performed by on-chip data processing resources of the emulation ICs. **Vries et al.** teaches that at least some of the generation of testing stimuli are performed by on-chip data processing resources of the emulation ICs (Page 353, CL1, Para 4, L3-5; Page 353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **Quayle et al.** with the method of **Vries et al.** that included at least some of the generation of testing stimuli being performed by on-chip data processing resources of the emulation ICs. The artisan would have been motivated because the amount of test data to be processed by the tester would be reduced by means of on-chip processing reducing the overall test time; and that would reduce the test costs of an IC design.

8.5 As per claim 19, **Quayle et al.** teaches an emulation system (Fig. 12; CL18, L26-31), comprising:

a plurality of logic boards (Fig. 12; CL18, L26-31), each having a plurality of emulation integrated circuits (IC) including reconfigurable logic and interconnect resources reconfigurable

to emulate circuit elements of partitions of an IC design (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13), and on-board data processing resources to locally and correspondingly generate testing stimuli, and apply the generated stimuli to the emulated circuit elements of the partitions of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to testing requests received through input/output (I/O) pins of the logic boards (Fig. 19, BP clocks); and

a workstation coupled to the logic board, including electronic design automation (EDA) software (CL23, L29-31; C26, L10-13; Fig. 20, Item 700), to provide the logic boards with the testing requests (Fig. 19, BP clocks).

Quayle et al. does not expressly teach that at least one of the emulation ICs of the logic boards comprises on-chip data processing resources to cooperate with and assist the on-board data processing resources of the logic board to perform the local and corresponding generation and application of testing stimuli. **Vries et al.** teaches that at least one of the emulation ICs of the logic boards comprises on-chip data processing resources to cooperate with and assist the on-board data processing resources of the logic board to perform the local and corresponding generation and application of testing stimuli (Page 353, CL1, Para 4, L3-5; Page 353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the emulation system of **Quayle et al.** with the emulation system of **Vries et al.** that included at least one of the emulation ICs of the logic

boards comprising on-chip data processing resources to cooperate with and assist the on-board data processing resources of the logic board to perform the local and corresponding generation and application of testing stimuli. The artisan would have been motivated because the amount of test data to be processed by the tester would be reduced by means of on-chip processing reducing the overall test time; and that would reduce the test costs an IC design.

Per claim 20: **Quayle et al.** teaches that the on-board data processing resources of each of the logic board comprise storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the local and corresponding generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

8.6 As per claim 24, **Quayle et al.** teaches in an emulation system, a method of operation (Fig. 12; CL18, L26-31), comprising:

locally and correspondingly generating testing stimuli; and locally and corresponding applying the generated testing stimuli to selected ones of the emulation circuit elements of emulation ICs corresponding to respective partitions of an IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

Quayle et al. does not expressly teach that at least some of the performances of local and corresponding generation and application of testing stimuli are assisted by on-chip data processing resources of the emulation ICs of the logic boards. **Vries et al.** teaches that at least

some of the performances of local and corresponding generation and application of testing stimuli are assisted by on-chip data processing resources of the emulation ICs of the logic boards (Page 353, CL1, Para 4, L3-5; Page 353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **Quayle et al.** with the method of **Vries et al.** that included at least some of the performances of local and corresponding generation and application of testing stimuli being assisted by on-chip data processing resources of the emulation ICs of the logic boards. The artisan would have been motivated because the amount of test data to be processed by the tester would be reduced by means of on-chip processing reducing the overall test time; and that would reduce the test costs an IC design.

8.7 As per claim 30, **Quayle et al.** teaches in an emulation integrated circuit (IC), a method of operation (CL1, L24-33), comprising

locally retrieving on the emulation IC, using on-chip data processing resources, state data of emulation state circuit elements of the emulation IC corresponding to a partition of an IC design being emulated (CL18, L5-9; CL23, L63-65);

locally analyzing the state data of the emulation state circuit elements, using on chip data processing resources, to detect occurrence of one or more events; and reporting on occurrence of the one or more events upon detecting their occurrence (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Quayle et al. does not expressly teach locally generating testing stimuli using the on-chip data processing resources; and locally applying the generated testing stimuli to an IC design being emulated, using the on-chip data processing resources. **Vries et al.** teaches locally generating testing stimuli using the on-chip data processing resources; and locally applying the generated testing stimuli to an IC design being emulated, using the on-chip data processing resources (Page 353, CL1, Para 4, L3-5; Page 353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **Quayle et al.** with the method of **Vries et al.** that included locally generating testing stimuli using the on-chip data processing resources; and locally applying the generated testing stimuli to an IC design being emulated, using the on-chip data processing resources. The artisan would have been motivated because the amount of test data to be processed by the tester would be reduced by means of on-chip processing reducing the overall test time; and that would reduce the test costs an IC design.

8.8 As per claim 32, **Quayle et al.** teaches an emulation integrated circuit (IC) (CL1, L24-33), comprising

a plurality of reconfigurable logic and interconnect resources configured to form emulation circuit elements corresponding to a partition of an IC design being emulated (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13).

Quayle et al. does not expressly teach on-chip data processing resources coupled to the reconfigurable logic and interconnect resources to locally generate testing stimuli, and locally apply the generated testing stimuli to at least one of the emulation circuit elements. **Vries et al.** teaches on-chip data processing resources coupled to the reconfigurable logic and interconnect resources to locally generate testing stimuli, and locally apply the generated testing stimuli to at least one of the emulation circuit elements (Page 353, CL1, Para 4, L3-5; Page 353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the emulation integrated circuit of **Quayle et al.** with the emulation integrated circuit of **Vries et al.** that included on-chip data processing resources coupled to the reconfigurable logic and interconnect resources to locally generate testing stimuli, and locally apply the generated testing stimuli to at least one of the emulation circuit elements. The artisan would have been motivated because the amount of test data to be processed by the tester would be reduced by means of on-chip processing reducing the overall test time; and that would reduce the test costs an IC design.

Per claim 33: **Quayle et al.** teaches that the on-chip data processing resources comprises a storage medium having stored therein programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), designed to

perform the local generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

8.9 As per claim 34, **Quayle et al.** teaches in an emulation integrated circuit (IC) (CL1, L24-33), a plurality of reconfigurable logic and interconnect resources configured to form emulation circuit elements corresponding to a partition of an IC design being emulated (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13).

Quayle et al. does not expressly teach the method of operation comprising locally generating on the emulation IC testing stimuli, using on-chip data processing resources; and locally applying the testing stimuli, using the on-chip data processing resources, to at least one of the emulation circuit elements. **Vries et al.** teaches the method of operation comprising locally generating on the emulation IC testing stimuli, using on-chip data processing resources; and locally applying the testing stimuli, using the on-chip data processing resources, to at least one of the emulation circuit elements (Page 353, CL1, Para 4, L3-5; Page 353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **Quayle et al.** with the method of **Vries et al.** that included the method of operation comprising locally generating on the emulation IC testing stimuli, using on-chip data processing resources; and locally applying the testing stimuli, using the on-chip data processing resources, to at least one of the emulation

circuit elements. The artisan would have been motivated because the amount of test data to be processed by the tester would be reduced by means of on-chip processing reducing the overall test time; and that would reduce the test costs an IC design.

Response to Arguments

9. Applicant's arguments filed on June 10, 2005 have been fully considered. The arguments with respect to 102 (b) rejections of Claims 1-34 are moot in view of the new ground(s) of rejection which are applied against the amended claims.

9.1 As per the applicant's argument that "**Quayle et al.** do not teach on-chip data processing resources used to generate and/or apply emulation IC testing stimulii", the examiner has used a new reference **Vries et al.**

Vries et al. teaches that at least one of the emulation ICs comprises on-chip data processing resources to cooperate and assist the onboard data processing resources to perform the local generation and application of testing stimuli (Page 353, CL1, Para 4, L3-5; Page 353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9).

Vries et al. teaches that at least some of the generation of testing stimuli are performed by on-chip data processing resources of the emulation ICs (Page 353, CL1, Para 4, L3-5; Page

353, CL2, P1, L1-3 and L11-13), because the amount of test data to be processed by the tester will be reduced by means of on-chip processing reducing the overall test time; and that will reduce the test costs of an IC design (Page 353, CL2, L1-9).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
August 17, 2005